

01-07-05

AF/2815/m

Attorney's Docket No. 67,200-409

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JAN 05 2005

PATENT & TRADE

In re application of: Chou et al

Serial No.: 09/978,420

Filed: Oct. 15, 2001

For: Microelectronic Fabrication With Upper Lying aluminum Fuse Layer in Copper Interconnect Semiconductor Technology and Method for Fabrication Thereof

Group Art Unit: 2815

Examiner: N. Drew Richards

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF REVISED APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on Sept. 8, 2004.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT

This application is on behalf of:

other than a small entity.
 a small entity.

A verified statement:

is attached.
 was already filed.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

small entity
 other than a small entity

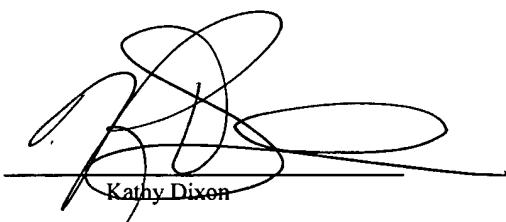
REVISED Appeal Brief fee due: \$ 0

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for Patents, Alexandria, VA 22313


Kathy Dixon

Dated: Jan. 5, 2005

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of 1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) Applicant petitions for an extension of time under 37 CFR 1.136
(fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

Extension (months)	Fee for other than <u>small entity</u>	Fee for <u>small entity</u>
<input type="checkbox"/> one month	\$ 110.00	\$ 55.00
<input type="checkbox"/> two months	\$ 430.00	\$215.00
<input type="checkbox"/> three months	\$ 980.00	\$490.00
<input type="checkbox"/> four months	\$1,530.00	\$765.00

Fee: \$

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

An extension for _____ months has already been secured, and the fee paid therefor of \$ _____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: \$

or

(b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: \$ 00
Extension fee (if any) \$ _____

TOTAL FEE DUE: \$ 00

6. FEE PAYMENT

— Attached is a Credit Card Payment Form for the sum of \$ 00

A duplicate copy of this transmittal is attached.

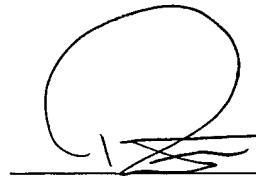
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

If any additional extension and/or fee is required, this is a request therefor to charge Deposit Account No. 50-0484

And/Or

If any additional fee for claims is required, please charge Deposit Account No. 50-0484



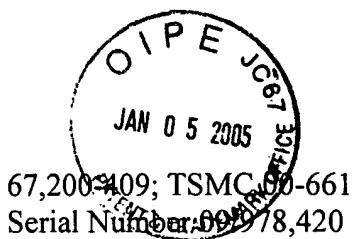
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FROM: Tung & Associates
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Bloomfield Hills, MI 48302

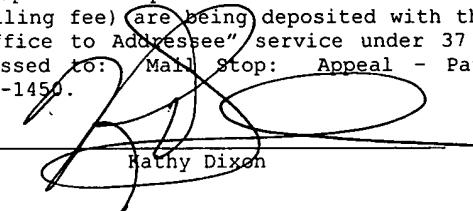
DATE: 22 December 2004

REF: Appellant : Chou et al Filing Date : 15 October 2001
Serial No. : 09/978,420 Atty No. : 67,200-409; TSMC 00-661
Art Unit : 2815 Examiner : N. Drew Richards
Title : Microelectronic Fabrication With Upper Lying Aluminum Fuse
Layer in Copper Interconnect Semiconductor Technology and
Method for Fabrication Thereof

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 510 274 515 US
Date of Deposit Jan. 5/05

I hereby certify that this paper in triplicate and a credit card payment form in the amount of \$330.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal - Patent, Commissioner for Patents, Alexandria, Va 22313-1450.



Kathy Dixon

REVISED APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 8 June 2004 and made FINAL, appellant filed a notice of appeal on 8 September 2004. Applicant filed a non-compliant appeal brief on 8 November 2004. This revised appeal brief addresses non-compliance issues enumerated by the Examiner in a notification of non-compliant appeal brief mailed 10 December 2004. In accord with appellant's original notice of appeal, please accept this revised appeal brief. No oral argument is requested.

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 1-3, 6 and 13 are pending in this application. Claims 4-5 and 7-12 have been canceled. No claims have been allowed, objected to or subject to restriction. Claims 1-3, 6 and 13 are finally rejected under 35 U.S.C. § 103(a). Appeal is taken for claims 1-3, 6 and 13 as finally rejected under 35 U.S.C. § 103(a).

4. Status of the Amendments

A reply, filed 9 August 2004, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 31 August 2004, the Examiner indicated that appellant's response was considered but did not place appellant's application in condition for allowance, for reasons related to those of record.

5. Summary of Claimed Subject Matter

The invention provides a microelectronic fabrication with enhanced access to a fuse layer within the microelectronic fabrication. (paragraph 0019)

The invention realizes the foregoing object by forming the fuse layer at a level no lower than a highest of a series of patterned conductor layers within the microelectronic fabrication. Thus, the fuse layer is provided with enhanced access and actuation. (paragraph 0020)

The invention is claimed in two levels of scope. Claim 1 and dependent claims 2-3 and 6 (group I) provide a method for fabricating a microelectronic fabrication where a fuse layer and the highest of the series of patterned conductor layers are formed of different conductor materials. Claim 13 (group II) provides a method for fabricating a microelectronic fabrication where a fuse layer is formed simultaneously with a bond pad and an alignment mark within the microelectronic fabrication.

The claims do not stand or fall together within their respective groups. In accord with argument below applicant asserts independent patentability of dependent claim 3 with respect to independent claim 1.

Independent claim 1, dependent claim 3 and independent claim 13 are read on the specification and drawings as follows:

1. (previously presented) A method for fabricating a microelectronic fabrication comprising:
 - providing a substrate 10; (Fig. 1 and paragraph 0031)
 - forming over the substrate 10 a series of patterned conductor layers 14a/14b/14c/14d/14e separated by a series of dielectric layers 12; (Fig. 1 and paragraph 0031) and
 - forming over the substrate 10 in electrical connection with the series of patterned conductor layers 14a/14b/14c/14d/14e separated by the series of dielectric layers 12 at least one fuse layer 18b formed simultaneously with an alignment mark 18a, wherein the at least one fuse layer 18b is formed at a level no lower than a highest of the series of patterned conductor layers 14a/14b/14c/14d/14e and wherein the at least one fuse layer 18b and the highest of the series of

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patterned conductor layers 14a/14b/14c/14d/14e are formed of different conductor materials. (Fig. 4; and paragraphs 0026 and 0048)

3. (original) The method of claim 1 wherein the at least one fuse layer 18b is formed simultaneously with a bond pad layer 18c within the microelectronic fabrication. (Fig. 4 and paragraph 0048)

13. (previously presented) A method for fabricating a microelectronic fabrication comprising:
providing a substrate 10; (Fig. 1 and paragraph 0031)
forming over the substrate 10 a series of patterned conductor layers 14a/14b/14c/14d/14e separated by a series of dielectric layers 12; (Fig. 1 and paragraph 0031) and
forming over the substrate 10 in electrical connection with the series of patterned conductor layers 14a/14b/14c/14d/14e separated by the series of dielectric layers 12 at least one fuse layer 18b, wherein the at least one fuse layer 18b is formed at a level no lower than a highest of the series of patterned conductor layers 14a/14b/14c/14d/14e and wherein the at least one fuse layer 18b is formed simultaneously with an alignment mark 18a and a bond pad 18c within the microelectronic fabrication. (Fig. 4 and paragraph 0048)

6. Ground of Rejection to be Reviewed on Appeal

Whether claims 1-3, 6 and 13 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 20020155672 A1; hereinafter "Wang") in view of Koike (U.S. Patent No. 6,392,300).

7. Argument

I. The claims do not stand or fall together within their respective groups.

With respect to group I, claims 1-3 and 6, appellant requests specific consideration of appellant's claim 3 that provides that appellant's at least one fuse layer is formed simultaneously with a bond pad and an alignment mark within appellant's

microelectronic fabrication. In accord with further argument below, appellant asserts that at least this feature of appellant's claimed invention is novel and provides for patentability of appellant's claimed invention.

II. Claims 1-3, 6 and 13 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Koike.

a. Wang Subject Matter

Wang (Fig. 3 and paragraph 0019) discloses a microelectronic fabrication having a bond pad 112b (right hand side connected to patterned conductor layer 102) and a series of fuse layers 112b (left hand side) formed simultaneously therein.

b. Koike Subject Matter

Koike (Fig. 6 and col. 2, lines 12-20) teaches a microelectronic fabrication having an alignment mark 27A and a bonding pad 27B formed simultaneously therein.

c. The Examiner's Assertions

Within the paragraph bridging pages 2-3 of the office action made FINAL, the Examiner reads Wang onto appellant's claim 1. The Examiner at page 3, second full paragraph and page 5, third full paragraph of the office action made FINAL acknowledges that Wang does not teach a fuse layer formed simultaneously with an alignment mark within a microelectronic fabrication. Rather, the Examiner at page 3, third full paragraph and paragraph bridging pages 5-6 of the office action made FINAL cites Koike for teaching that an alignment mark 27A may be formed simultaneously with a fuse layer (not shown) or a bond pad 27B within a microelectronic fabrication.

The Examiner at the paragraph bridging pages 3-4 and page 6, first full paragraph of the office action made FINAL first rationalizes suggestion or motivation for modification or

combination of Wang and Koike upon the assertion that they are in the same field of endeavor. The Examiner also rationalizes suggestion or motivation for providing Koike's alignment mark and a fuse formed simultaneously in an upper metal layer within Wang's microelectronic fabrication so that the alignment mark may be employed for positioning a laser when severing the fuse, apparently in accord with Koika at col. 2, lines 21-28.

Within the advisory action, the Examiner further responds with specificity to appellant's responses to the Examiner's above assertions. Appellant addresses these additional responses within the context of appellant's response, below.

d. Appellant's Response

In response in a first instance, appellant first notes that the Examiner acknowledges that Wang does not disclose an alignment mark formed simultaneously with a fuse layer and a bond pad within a microelectronic fabrication. In addition, while Koike at Fig. 5 and col. 2, lines 1-11 does teach an alignment mark 27A formed simultaneously with a bond pad 27B, Koike further teaches that "a metal fuse (not shown) or a bonding pad 27B is formed from a part of the fourth aluminum layer." (emphasis added) In addition Koike also teaches that "[a]n alignment mark 27A is also formed from part of the fourth aluminum layer." Thus, Koike apparently explicitly teaches that only either a bond pad or a fuse layer is formed simultaneously with an alignment mark, but not both a bond pad and a fuse layer are formed simultaneously with the alignment mark.

Appellant within claim 3 and claim 13 explicitly claims the simultaneous formation of a bond pad, a fuse layer and an alignment mark. However, each of the prior art references explicitly teaches simultaneous formation of only two of those components. Wang teaches simultaneous formation of a fuse layer and a bond pad with no mention of an alignment mark. Koike teaches simultaneous formation of alignment mark with either a fuse layer or a bond pad. Thus, Koike implicitly teaches that an alignment mark may not be formed when both

a fuse layer and a bond pad are present. This provides a result consistent with Wang. A person skilled in that art at the time of appellant's invention might plausibly conclude that only two of a fuse layer, a bond pad and an alignment mark may be formed simultaneously, since the prior art appears to explicitly provide for only that result.

"A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." MPEP 2141.02 (citing *W.L. Gore and Associates, Inc. v. Garlock, Inc.* (citation omitted)).

"[T]he prior art reference (or references when combined) must teach or suggest all of the claim limitations." MPEP 2143.

Thus, since: (1) each and every limitation within appellant's invention as disclosed and claimed within claim 3 and claim 13 is not taught within Wang, Koike or the combination thereof with respect to all three of a fuse layer, a bond pad and an alignment mark being formed simultaneously within a microelectronic fabrication; and (2) at least Koike apparently teaches away from that result, appellant asserts that claim 3 and claim 13 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Koike.

In light of the foregoing response, appellant respectfully requests that the Examiner's rejections of claims 3 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Koike be reversed.

With respect to the foregoing response, the Examiner within the advisory action accurately further responds that "[t]he issue at hand is whether Koike in using the term 'or' (column 6, lines 24-27) has explicitly taught that the fuse and the bond pad can not both be formed simultaneously with an alignment mark." In accord with appellant's above response,

appellant clearly asserts that “or” is intended by Koike as mutually exclusive with respect to formation of either one of a bond pad and a fuse layer with an alignment mark. In contrast, the Examiner apparently asserts otherwise, and that “or” as employed by Koike is not intended as “ONLY one of [Koike’s] bond pad and [Koike’s] fuse layer is formed” simultaneously with Koike’s alignment mark.

Appellant appreciates that the Examiner has accurately framed the issue with respect to appellant’s and the Examiner’s reading of Koike, and the resulting conflicting interpretations of Koike’s intention for use of the word “or.” Appellant continues to assert that “or” as employed by Koike is limited to its common usage since Koike does not specify otherwise. In common usage “or” is clearly limited to only one of at least a pair of options (i.e., A or B, or in the instant application a bond pad or a fuse layer) since if Koike had intended more than one of the pair of options Koike could easily have employed alternative common terminology to achieve that end (i.e., A and/or B, or in the instant application a bond pad and/or a fuse layer).

In light of appellant’s further response, appellant continues to respectfully request that the Examiner’s rejections of appellant’s claims 3 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Koike be reversed.

In response in a second instance, appellant asserts that Wang and Koike may not properly be combined to provide appellant’s claimed invention incident to the Examiner’s first rationale directed toward their mere existence in the same field of endeavor, since the same provides an insufficient basis to establish *prima facie* obviousness.

“The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.” MPEP 2143.01 (citing *In re Mills* (citation omitted)).

In accord with *In re Mills*, proper modification or combination of references requires that the suggestion or motivation for such modification or combination be found within the prior art references themselves. In contrast, the fact that a pair of references may be in the same field of endeavor, as observed by an Examiner, does not impute into the references a suggestion or motivation for modification or combination to provide an appellant's claimed invention.

For purposes of illustration, a pair of references may clearly be in the same field of endeavor. However, it is also plausible that each of the pair of references teaches away from the other of the pair of references such that upon combination in a fashion as suggested by an Examiner a principal of operation of a base reference is changed or it is otherwise rendered unsatisfactory for its intended purpose. MPEP 2143.01. Under such circumstances, the references are clearly not combinable although they are in the same field of endeavor. Thus, it is the teachings of the references themselves, and not their mere existence in the same field of endeavor, that must be evaluated for purposes of suggestion or motivation for modification or combination of references. Absent a recognition and analysis of such teachings references may not properly be combined to reject any of an appellant's claims to the appellant's invention under 35 U.S.C. § 103(a).

In light of the foregoing response, appellant respectfully requests that the Examiner's rejections of appellant's claims to appellant's invention under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Koike incident to the Examiner's first rationale for combination thereof be reversed.

In response in a third instance, appellant asserts that the Examiner's second rationalization for suggestion or motivation for modification or combination of Wang with Koike, while apparently applicable to a specific situation taught within Koike, is not necessarily

applicable to Wang. For this reason also, appellant additionally asserts that no suggestion or motivation for modification or combination of Wang with Koike exists.

In that regard, the Examiner's second rationalization is apparently predicated upon a teaching within Koike at col. 2, lines 25-28 that "[i]f the alignment mark 27A is removed, fuse-blow cannot be performed, since the alignment mark 27A, for use in positioning the laser when the fuse is blown, cannot be detected." Thus, the Examiner apparently concludes that a suggestion or motivation for modification or combination of Wang (teaching a series of fuse layers and a bond pad formed simultaneously) by including Koike (teaching an alignment mark formed simultaneously with a fuse layer) is predicated upon Koike's teaching of a need for an alignment mark for positioning a laser when severing a fuse layer.

For comparison purposes, appellant notes that Wang at paragraph 0021 teaches that "a passivation layer 118 is formed over the substrate 100 exposing just the bonding pad 112a and the metal fuses 112b." Thus, in addition to being silent with regard to the presence of an alignment mark formed simultaneously with a fuse layer and a bond pad, it might also be explicit or at least implicit within Wang that Wang does not form any other layers simultaneously with Wang's bonding pad 112a and metal fuses 112b, but rather "just the bonding pad 112a and the metal fuses 112b." Had Wang simultaneously formed an alignment mark, the same would also have clearly been exposed for proper alignment purposes that are suggested as needed by the Examiner.

With respect to a variant of the above response, the Examiner within the advisory action further asserts in part that "Wang's lack of teaching the passivation layer exposing the alignment mark is not an implicit statement that an alignment mark can not be formed in their device."

Appellant appreciates and understands the Examiner's apparent position that, in general, a lack of teaching of an element within a claimed invention is not an implicit statement that the claimed element cannot be formed within the invention. However, the Examiner appears to be applying a general rule to Wang, absent full consideration of the specifics of Wang's teachings. Wang clearly teaches that just a fuse layer and a bond pad are exposed by a passivation layer. Due to this teaching, Wang might reasonably be interpreted as apparently explicit as to absence of other exposable structures formed within Wang's microelectronic fabrication. These other exposable structures might plausibly implicitly include alignment marks. Thus, while a general rule that lack of teaching of an element within an invention is not an implicit statement that the element cannot be formed within the invention, a specific teaching of presence of only certain elements may reasonably be interpreted as explicit or implicit as to absence of other elements.

Applicant is unable to conjecture with certainty as to how Wang positions a laser to sever one of Wang's fuses. However, Wang clearly excludes and does not require an alignment mark formed at an identical level to effect such a result since Wang has explicitly taught otherwise. As pure conjecture, perhaps Wang might employ an alignment mark formed at a lower level, or in an alternative perhaps one of Wang's fuse layers may be employed as an alignment mark.

Thus, since the Examiner's second rationale for suggestion or motivation for modification or combination of Wang with Koike is not apparently applicable to Wang, appellant asserts that Wang may not properly be combined with Koike for reasons in accord with the Examiner's second rationale. For this reason also, appellant asserts that none of appellant's claims to appellant's invention may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Koike, for reasons as advanced by the Examiner.

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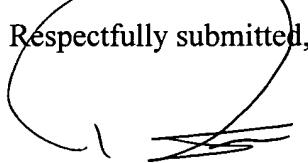
In light of the foregoing responses, appellant's respectfully requests that the Examiner's rejections of claims 1-3, 6 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Koike be reversed.

8. Summary

Appellant's invention as disclosed and claimed within claim 3 and claim 13 is directed towards a method for fabricating a microelectronic fabrication having formed therein a series of patterned conductor layers and a fuse layer. Within appellant's invention, the fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers. Within the invention, the at least one fuse layer is formed simultaneously with a bond pad and an alignment mark within the microelectronic fabrication. Absent from the prior art of record employed in rejecting appellant's claims to appellant's invention is a teaching of each and every limitation within appellant's invention, or a suggestion or motivation to modify or combine references to provide appellant's claimed invention.

9. Conclusion

Appellant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims pending within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,


Randy W. Tung (Reg. No. 31,311)

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APPENDIX I
CLAIMS APPENDIX

1. (previously presented) A method for fabricating a microelectronic fabrication comprising:
 - providing a substrate;
 - forming over the substrate a series of patterned conductor layers separated by a series of dielectric layers; and
 - forming over the substrate in electrical connection with the series of patterned conductor layers separated by the series of dielectric layers at least one fuse layer formed simultaneously with an alignment mark, wherein the at least one fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers and wherein the at least one fuse layer and the highest of the series of patterned conductor layers are formed of different conductor materials.
2. (original) The method of claim 1 wherein the microelectronic fabrication is selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.
3. (original) The method of claim 1 wherein the at least one fuse layer is formed simultaneously with a bond pad layer within the microelectronic fabrication.
4. – 5. (canceled)
6. (original) The method of claim 1 wherein the at least one fuse layer is formed of an aluminum containing conductor material and the highest of the series of patterned conductor layers is formed of a copper containing conductor material.

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7. - 12. (canceled)

13. (previously presented) A method for fabricating a microelectronic fabrication comprising:
 providing a substrate;
 forming over the substrate a series of patterned conductor layers separated by a series of dielectric layers; and
 forming over the substrate in electrical connection with the series of patterned conductor layers separated by the series of dielectric layers at least one fuse layer, wherein the at least one fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers and wherein the at least one fuse layer is formed simultaneously with an alignment mark and a bond pad within the microelectronic fabrication.

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APPENDIX II
EVIDENCE APPENDIX

None

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APPENDIX III
RELATED PROCEEDINGS APPENDIX

None